Ilorin Journal of Science
Volume 2, Number 1, 2015, pp. 34 – 47 (Printed in Nigeria)
ISSN: 2408 – 4840 © 2015 Faculty of Physical Sciences, University of Ilorin
https://doi.org/10.54908/iljs.2015.02.01.004

ILORIN
JOURNAL OF SCEINCE

ILJS-15-054

Fabrication of Advanced High-Speed Complementary Metal Oxide Semiconductor Field Effect Transistor

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Abstract

In this study we propose the fabrication of advanced high-speed complementary metal oxide semiconductor field effect transistor (AHCMOS) by combining a P-carbon nanotube with n-metal oxide semiconductor (NMOS) on a single chip. The target is to achieve extremely high speed low-power dissipating miniaturized device with improved functionalities. The technology of conventional metal oxide semiconductor field effect transistor (MOSFET) and nanotechnology are applied in this research. A P-carbon nanotube is complemented with the conventional NMOS all embedded on the same chip. Although it is possible to fabricate both a P and N carbon nanotube to form a complementary pair, and also a PMOS and NMOS to form a complementary pair, however in this research we propose a hybrid structure with carbon nanotube transistor technology and complementary MOSFET technology. This device therefore combines the best characteristics of carbon nanotube technology and CMOS technology to provide enhanced logic functions that are optimized for the high-speed, low-power systems and miniaturized size ideal for very large scale integration (VLSI).

Keywords: Carbon Nanotube, Nanotechnology, CMOS, MOSFET, Integrated Circuit.

1. Introduction

The speed-power product is a figure of merit for integrated circuit families. Transistors have evolved from bipolar junction transistors with high-speed high-power consumption to field effect transistors with low-speed low-power consumption. One advantage that MOSFETs have over bipolar transistors is that the input to a MOSFET is electrically isolated from the device (Mehta, 2008; Schichman, 1968). This gives high input impedance thus reducing the input current and power dissipation. However, the bipolar transistor offers high speed of operation especially the Schottky transistors. A combination of a PMOS and NMOS on a single chip produces a CMOS with low-power high-speed operation. The PMOS is adversely affected by negative-bias temperature instability (NBTI) which consequently decreases the drain current and the composite transconductance of a CMOS (Alam, 2005).

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Performance requirements for higher speed levels and larger transconductance, motivated a switch from CMOS to BiCMOS (Bipolar Complementary Metal Oxide Semiconductors) in 1980's (Neamen, 1996; Ferlet-Cavrois, 2013). The BiCMOS suffers two fundamental limitations namely poor voltage scalability and poor speed improvement (Tsividis, 1999). The BiCMOS circuit has a longer composite transconductance compared to the MOSFET. It has the advantage of large transconductance and infinite input resistance derived from the bipolar junction transistor and MOSFET respectively. The fact that a base-emitter voltage of approximately 0.8V is required for a fast turn-on imposes a lower limit of about 2.0-2.5V on the supply voltage. Also the speed of bipolar devices does not scale as fast compared to the size of CMOS.

In this research the efficiency and size of the complementary metal oxide semiconductor field effect transistor has been improved. The advantages of applying the P-Carbon Nanotube are merged with the conventional NMOS to form a heterostructure targeted at overcoming the limitations of the BiCMOS and eliminating the effect of degradation associated with N-Carbon nanotube. Carbon nanotubes offer unique electronic structure as it can be rolled up to form a hollow cylinder with the circumference expressed in order of its chiral vector (Lortz, 2009; Charlier, 2007; Thostenson, 2005). Its crystallographic equivalent of two dimensional grapheme tubes is expressed in equation 1.

$$\hat{C}_h = n\hat{a}_1 + m\hat{a}_2(1), \quad (1)$$

where n and m are integers and $\hat{a}_1$ and $\hat{a}_2$ are the unit vectors of the hexagonal lattice as shown in Figure 1A and 1B.

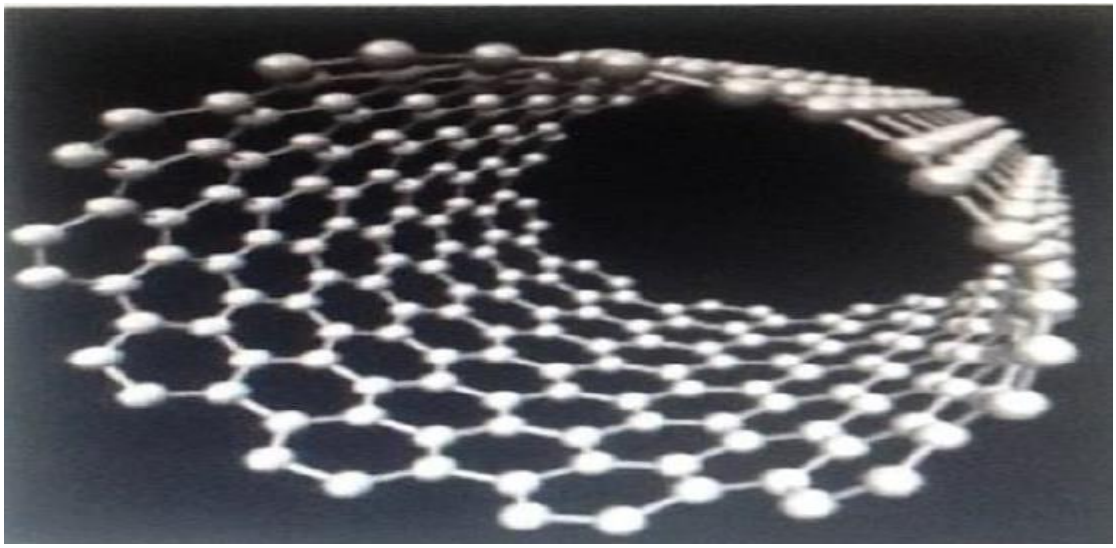

Fig. 1A: Hexagonal Lattice of a Carbon Nanotube

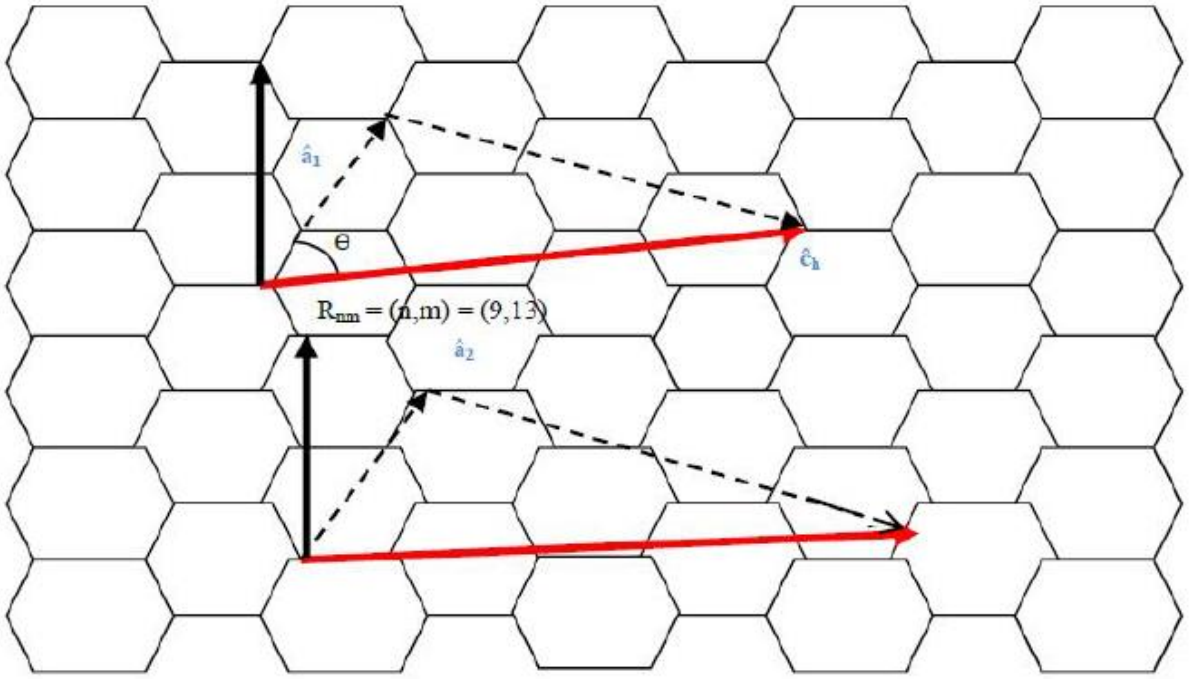

Fig. 1B: Hexagonal Atomic Structure of Graphene Showing the Chiral vector $\hat{C}_h$.

The properties of the carbon nanotube are determined by the chiral angle and its corresponding diameter of the circumference (Bertozzi, 2009; Gullapalli, 2011; Stoner, 2011). A carbon nanotube field effect transistor utilizes a single carbon nanotube or an array of carbon nanotubes as a channel material instead of bulk silicon in the conventional MOSFET structure. Applying the carbon nanotube technology allows further scaling down of the field effect device to sub 22nm range. At such nano scales, the MOSFET suffers major limitations with its operation due to the threshold involved in electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects and variation in device structure doping. These limits are overcome by the advanced high speed CMOS to achieve further scaling down of device dimensions through the integration of the channel material in the traditional bulk MOSFET structure with an array of carbon nanotubes.

2.1 Materials and Methods

The techniques for the fabrication of Carbon Nanotubes have evolved over the years. It started with the Back-gated technique with a lot of defects. This method involves the pre-patterning parallel strips of metal across a silicon dioxide substrate, and then randomly

depositing the CNTs on the surface. The result is that one metal is the source terminal and the other is the drain terminal while the silicon oxide substrate serves as the gate oxide. The limitations of this technique include very poor metal contact area for the terminals leading to formation of Schottky barrier at the metal semiconductor interface. Again, the thickness of the device does not allow the switching of the system using low voltages (Flahaut, 2003; Wang, 2009; Huhtala, 2002; Yu, 2011; Hsin-Cheng, 2012; Parker, 2012). Following these defects in the Back gated technique, the Top gated method was introduced. This involves the deposition of single walled carbon nanotubes solutions onto silicon oxide substrate.

Individual nanotubes are now isolated using Scanning Electron Microscope. By annealing with high temperature, a thin Top-gate dielectric is deposited on top of the nanotube by atomic layer deposition. The top contact is then deposited on the gate dielectric, achieving better area contacts and minimizing contact resistance. The thin gate dielectric also enables a larger electric field to be generated in the nanotube with very low gate voltage. In order to further increase the metal contact area, the Wrap-around gate CNFETs technique was developed in which the entire circumference of the nanotube is gated (Li, 2010; Jensen, 2007; Meo, 2000; Yang, 2011).

This technique involves the wrapping of the whole CNTs in a gate dielectric and gate terminal through the process of atomic layer deposition. This method was deployed in the fabrication of the n-CNTFET. It offers many advantages such as reduced leakage current, improved device on/off ratio and a better electrical performance of the device (Kim, 2012; Ishigami, 2000; Banerjee, 2008; Yamada, 2012; Murr, 2004; Ding, 2000; Hadden, 2000; Postma, 2000).

2.2 Theoretical Methodology

The nanotube diameter d_t and the chiral angle θ is expressed given the integers (n,m) in equations 2 and 3:

$$d_t = \frac{\sqrt{3ac} - c\sqrt{m^2 + mn + n^2}}{\pi}, \quad (2)$$

where the chiral angle θ is expressed as:

$$\theta = \tan^{-1}\left(\frac{\sqrt{3}n}{2m+n}\right). \quad (3)$$

A carbon nanotube described by (n,m) can be classified as: Zig-zag if either n = 0 or m = 0, Armchair if n = m and n, or m is not zero, Chiral if n ≠ m.

Since the carbon nanotube field effect transistor (CNTFET) utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of the inversion layer created by silicon in the conventional CMOS, the drain current can be determined from Fermi – Dirac probability distributions shown in equations 4, 5, 6, and 7.

$$N_s = \frac{1}{2}\int_{-\infty}^{+\infty} D(E)f(E - U_{SF})dE \,, \quad (4)$$

$$N_D = \frac{1}{2}\int_{-\infty}^{+\infty} D(E)f(E - U_{DF})dE \,, \quad (5)$$

where N_S = Source charges from density of positive velocity states.

N_D = Drain charges from density of negative velocity states.

D(E) = Density of states at the channel.

While U_{SF} and U_{DF} are terms expressed by:

$$D(E) = D_0 \frac{E}{\sqrt{E^2 - \left(E_g/2\right)^2}}\theta(E - E_g/2), \quad (6)$$

$$U_{SF} = E_F - qV_{SC} \,,$$

$$U_{DF} = E_F - qV_{SC} - qV_{DS} \,,$$

where V_{SC} is the self-consistent voltage and V_{DS} is the drain source voltage.

The drain current I_{DS} is described by the following:

$$I_{DS} = \frac{2qkT}{\pi\hbar}\left[F_0\left(\frac{U_{SF}}{kT}\right) - F_0\left(\frac{U_{DF}}{kT}\right)\right] \,, \quad (7)$$

where k = Boltzmann's constant, ħ = Planck's constant, *T* = Temperature, F_0 = Fermi – Dirac integral of order 0.

It has been observed that the n-CNTFET suffers degradation when exposed to oxygen (Tracy, 1996; Oku, 2000; Stoner, 2012; Sugime, 2013; Collins, 2000; Belluci, 2005). Although attempts have been made in the fabrication to prolong the lifetime by using different polymers and by covering the top gate, it still presents a challenge concerning its reliability.

The multi-channeled CNFETs last longer as the multiple channels can function even when some channels break down (Wong, 2011).

Part of the major considerations in the fabrication of a complementary MOSFET is that the n-channel and the p-channel devices must be electrically equivalent (Vestling, 1999). Consequently, the magnitude of the threshold voltages must be equal and the n-channel and p-channel conduction parameters must be equal. However, since the electron mobility μ_n and holes mobility μ_p are not equal, the design of complementary heterostructure requires precision engineering of the device to achieve a match between the NMOS and the P-CNTFET.

In an NMOSFET, the ideal current – voltage characteristics at the non-saturation region is described in equations 8 and 9.

$$i_D = k_n [2(V_{GS} - V_{Th}) V_{DS} - V^2_{DS}] , \quad (8)$$

where i_D is the drain current, V_{GS} is the gate source voltage, V_{Th} is the threshold voltage, V_{DS} is the drain source voltage, K_n is the conduction parameter for n channel

$$K_n = \frac{W\mu_n C_{ox}}{2L} \quad (9)$$

where W is the n channel width, μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area as described in Figure 3.

For the saturation region of NMOS, the ideal drain current is shown in the equation below:

$$i_D = k_n(V_{GS} - V_{Th})^2 . \quad (10)$$

So, the magnitude of the current in the NMOS is a function of the amount of charge in the inversion layer, which in turn is a function of the applied gate voltage (Coleman, 2006; Zheng, 2001; Martel, 1998). The threshold voltage is the applied voltage needed to create an inversion layer in order to turn on the transistor on enhance mode.

The conventional silicon MOS technology is combined with semiconducting carbon nanotube to create a heterostructure with improved functionalities. The p- carbon nanotube introduces a unique electronic structure that reduces carrier scattering caused by one-dimensional quantum confinement effect (Javey, 2000; Jean-Christophe, 2003; Matson, 2010). Recent studies have shown that both carbon nanotubes and GE/Si core shell nanowires demonstrated long carrier mean free paths at room temperature (Chen, 2016). Carbon nanotubes offer near ballistic channel transport and easy application of high –k gate insulator. The scaling of planar silicon

MOSFETs has reached its limit and can only be taken further by substituting the p type with a p carbon nanotube. In this research we propose the following parameters for the fabrication: A silicon doping of $N_A = 10^{19}cm^{-3}$, insulator thickness t_{ins} = 1 nm and a dielectric constant of K_{ins} = 4. The gate work functions are selected to produce the same threshold voltage V_T for the P-CNTFET and NMOS. A 0.4V power supply to be applied as required for high density systems.

Experimentally, we propose that single crystal silicon (Si substrates) with resistivity of 0.005 – 0.01Ωcm, are cleaned and coated with 120 nm of thermal SiO_2.Single wall nanotubes produced by Laser ablation and dispersed from a 1,2 – dichloroethane solution by spinning onto the substrates after mild sonication. Then the density of the solution is adjusted to yield approximately one CNT in an area of 5 x 5 μm^2. Ti source and drain electrodes should be patterned by electron-beam lithography and lift off. The separation between the source and drain should be kept at 200 – 300nm apart. Through horizontal monolithical integration, the NMOS and P-carbon nanotube is placed side-by-side on a semi insulating substrate. Interconnections can be made by conductors over the epitaxial layers as shown in figures 2-4. This hybrid technology is expected to produce a transconductance of about 13000 µS/µm.

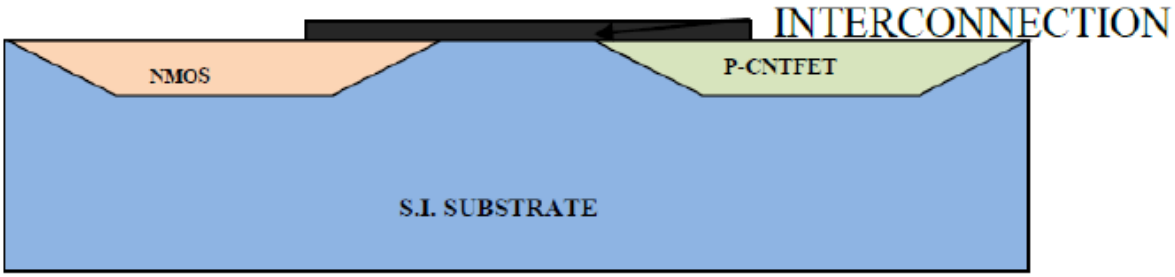

Fig. 2: Horizontal integration of NMOS with P-CNTFET

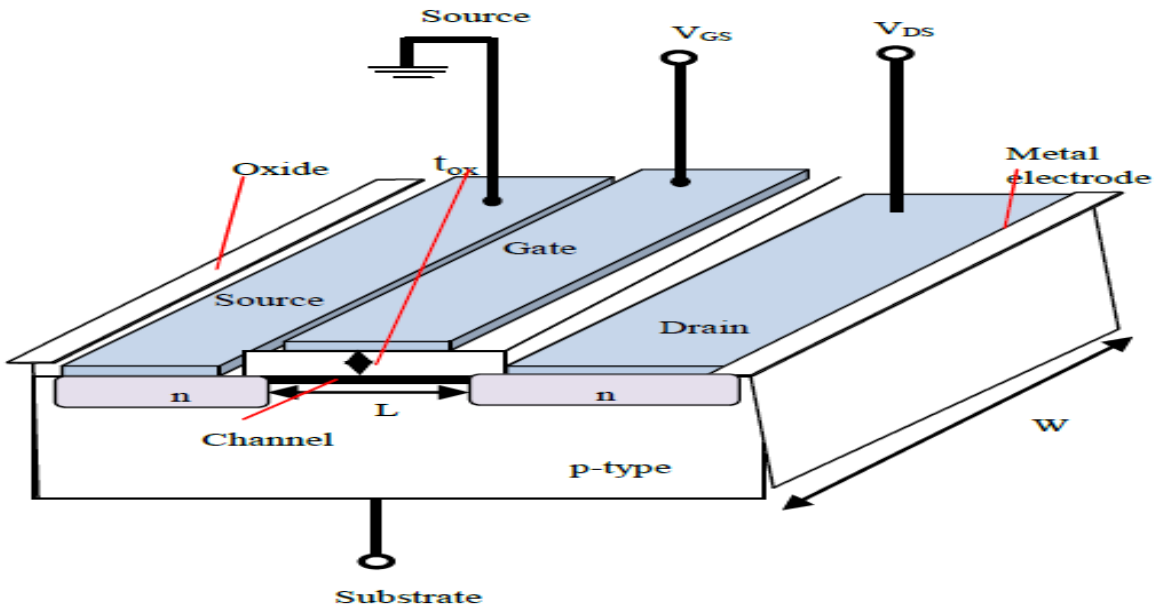

Fig. 3: N-Channel Enhancement Mode MOSFET

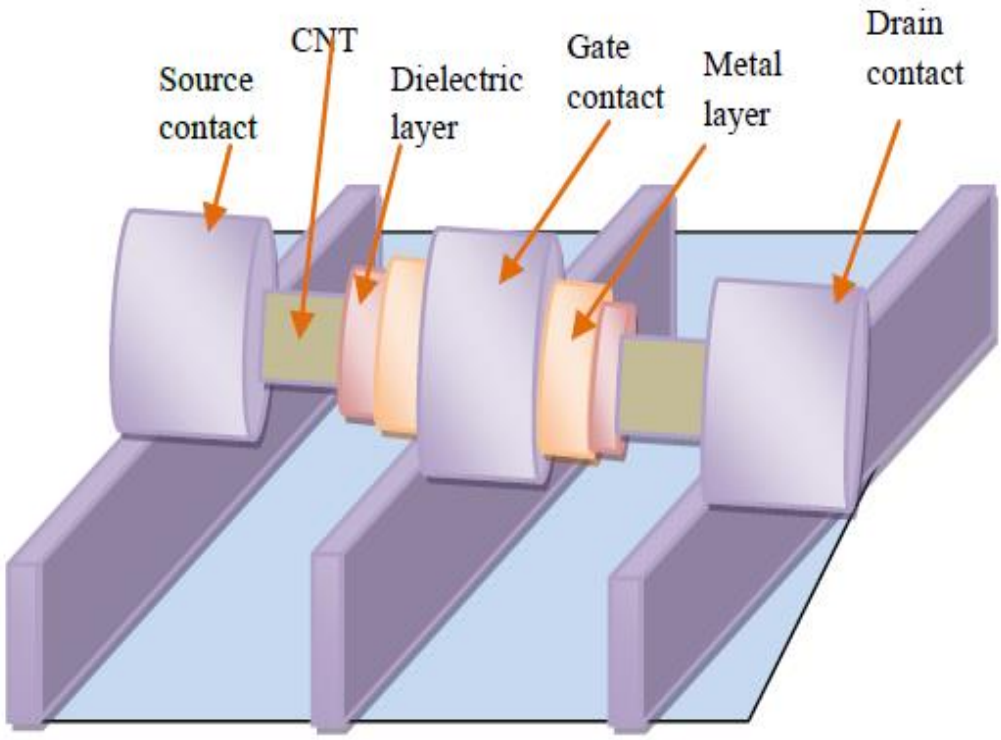

Fig. 4: P-CNTFET in Gate all-around contact

3. Results and Discussion

This proposed AHCMOS promises improved functionalities compared to the conventional CMOS, BiCMOS or CNTFET. The p-CNTFET under operational conditions produces

1850 A/m of the on-current per unit width at a gate override of 0.4 V. This is attributed to the high gate capacitance and improved channel transport introduced by the P-CNTFET. This proposed device transconductance is projected to increase as a result of higher drain-source current, on/off ratio and saturation properties.

The projected AHCMOS voltage transfer characteristics (VTC) are as shown in Figures 5 and 6 below.

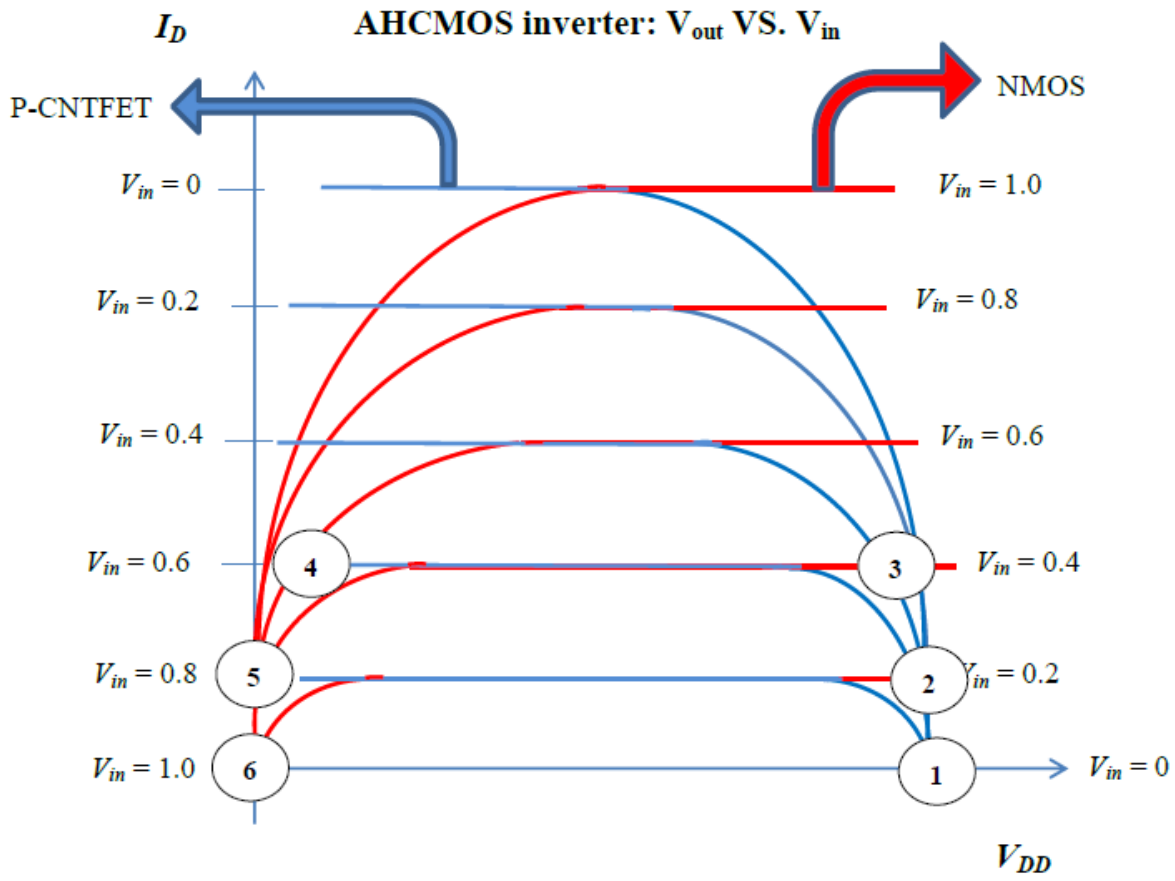

Fig. 5: AHCMOS Inverter Load Characteristics

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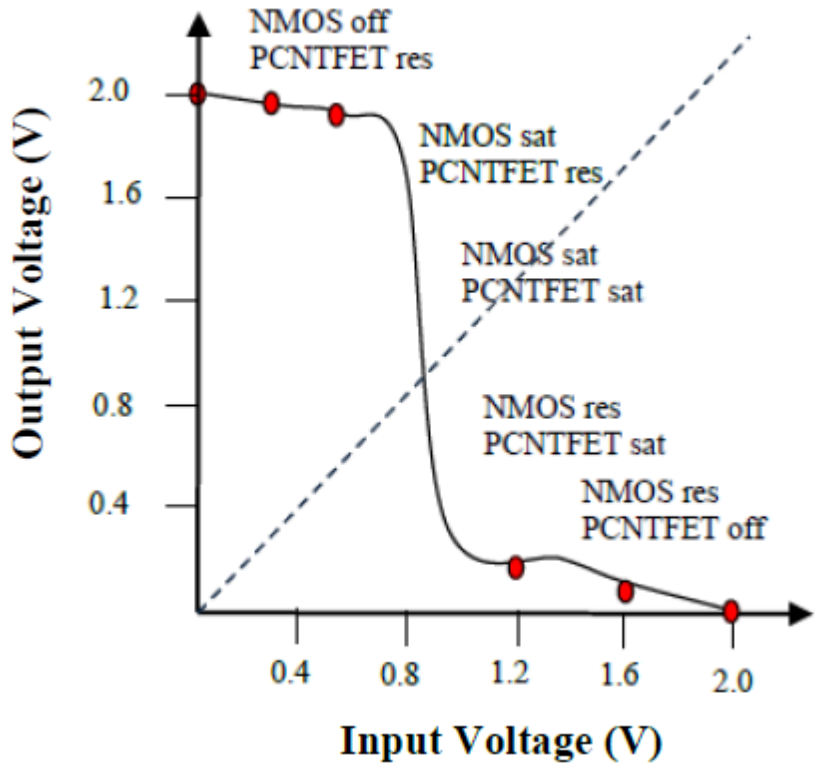

Fig. 6: Projected AHCMOS Inverter Voltage Transfer Characteristics

The voltage transfer characteristics represented in figure 5 outlines the output drain current I_D of both transistors. The drain currents of both transistors are made to be equal. Therefore, the intersection of the output characteristics of both transistors for each input voltage V_{in} give the output voltage V_{out}. The labeled circles mark five points of the voltage transfer characteristics. The mixed mode of Minimos-NT was used to simulate the whole circuit while the device characteristics for each field effect transistor device are solved using the semiconductor device equations. All operating points are located either high or low output levels creating a very narrow transient zone, thus high gain in transient. By using this technique, the degradation of the p-channel MOSFET due to negative bias temperature instability is now overcome through the use of PCNTFET. The transition from the On to the Off state is very aligned around $V_{DD}/2$ as shown in figure 6. The voltage transfer characteristics give the response of the inverter circuit, V_{out}, to specific input voltages, V_{in}. It is a figure of merit for the static behavior of this inverter. The gate-source voltage V_{GS} of the NMOS is equal to V_{in} while the gate-source voltage of the PCNTFET - V^P_{GS} was calculated using the equation:

$$V^P_{GS} = V_{in} - V_{DD} . \quad (11)$$

And the drain-source voltage V^P_{DS} of the PCNTFET is expressed as:

$$V^P_{DS} = V^n_{DS} - V_{DD,} \quad (12)$$

where V^n_{DS} is the drain-source voltage of the NMOS.

4. Conclusion

The AHCMOS hybrid technology of Carbon nanotube and Silicon MOSFET is very promising in the future of Nano-electronics. It presents a better control over channel formation, a better threshold voltage, desirable sub-threshold slope, impressive high carrier mobility, high current density, and excellent high composite transconductance. The negative-bias temperature instability (NBTI) which is usually associated with the PMOS is avoided by using the PCNTFET. The NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and transconductance of a MOSFET. The degradation exhibits logarithmic dependence on time. It is of immediate concern in PMOS devices since they most times operate with negative gate-to-source voltage. Furthermore, this hybrid technology is a welcome development towards creating opportunity for the mass production of this device at a reduced cost. A wafer-scale fabrication process with semiconductor contact materials using the dielectrophoresis technique is proposed. This device technology introduces further miniaturization of silicon CMOS at the nanometer geometry scale.

Acknowledgements

Our gratitude goes to the staff of Nano-laboratory, Optik Design, Technische Universitaet Ilmenau, Germany, for assisting in the laboratory fabrication works. Also to Prof. E.I.E.Ofodile, former Dean, Faculty of Engineering and Technology, Nnamdi Azikiwe University Awka, Nigeria, for all his guidance throughout this research project.

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